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3	U.S. Patent No. 8,977,797 (“797 patent”)
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6	U.S. Patent No. 7,363,416
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24	“National Semiconductor LVDS Owner’s Manual,” (1st Edition Spring 1997)
25	“National Semiconductor LVDS Owner’s Manual,” (2nd Ed. Spring 2000)
26	Huq, S., et al., “An Overview of LVDS Technology,” Application Note 971 (Jul. 1998)
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31	Ma, J., “A Closer Look at LVDS Technology,” Application Note 41
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44	Patent Owner’s Response, IPR2014-01462 (’873 Patent), Paper 30 (September 25, 2014)
45	PCI Local Bus Specification, Revision 2.2 (Dec. 18, 1998)
46	Universal Serial Bus Specification, Revision 2.0 (Apr. 27, 2000)
47	U.S. Patent No. 6,718,415
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58	<i>ACQIS LLC v. EMC Corp.</i> , 21-1772 (Fed. Cir.), Dkt. 35 (ACQIS Fed. Cir. Reply Br.)

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60	<i>ACQIS LLC v. EMC Corp.</i> , No. 1:14-cv-13560, Dkt. 189 (ACQIS Responsive CC Brief)
61	Patent Owner's Preliminary Response, IPR2021-01110 ('750 Patent), Paper 7 (September 17, 2021)
62	Institution Decision, IPR2021-01110 ('750 Patent), Paper 11 (Dec. 2, 2021)
63	U.S. Patent No. 7,558,326
64	U.S. Patent No. 7,502,411

**I. ACQIS IS PRECLUDED FROM RE-LITIGATING THE *EMC* CONSTRUCTIONS<sup>1</sup>**

ACQIS mischaracterizes prior proceedings and the familial relationship of its own patents to avoid the preclusive effects of the Federal Circuit’s express adoption of Defendants’ proposed constructions. ACQIS bases its preclusion arguments on the false notion that the *EMC* court did not consider claims reciting specific or certain bits of a PCI bus transaction.” Resp. Br., 4 (“[T]he *EMC* courts did not address the phrases at issue here [PCI bus transaction] reciting only certain bits of a ‘PCI bus transaction.’”), 5 (“Neither the *EMC* district court nor the Federal Circuit addressed phrases at issue in this case reciting the terms ‘encoded’ and/or ‘serial,’ which all recite *only specific bits* of a ‘PCI bus transaction.’”) (emphasis in original), 5 (“The phrase ‘communicating ... PCI bus transaction’ from *EMC*, without reference to specific recited bits being communicated, does not appear in any of the Asserted Claims here.”), 6 (“Neither the *EMC* district court nor the Federal Circuit addressed the claim language at issue here reciting specific bits of a ‘PCI bus transaction[.]’”). Plain and simple—this is false.

ACQIS’s briefing in *EMC* emphasized claims that recited “an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction.” Ex. 57 (ACQIS Surreply CC Br. in *EMC*) at 4-5 (reproducing claim 24 of ’171 patent and claim 48 of the ’984 patent). ACQIS likewise emphasized the importance of “Address and Data Claims” to the Federal Circuit, arguing that “[t]he Address and Data Claims should be treated separately,” and that there is no evidence that those claims “require generating a full PCI bus transaction (including control bits).” See Ex. 48 (ACQIS Appeal Reply Br.) at 17-21; see also Ex. 59 (ACQIS Corrected Appeal Br.) at 15-16 (noting that four of the claims at issue recite “address and data bits of a ... (PCI) bus transaction” (the ‘Address and Data Claims’)), 26 (arguing that Address and Data Claims “could

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<sup>1</sup> Defendant will address additional issue preclusion arguments with respect to specific claim terms below.

not require transmitting the address and data bits and also the control bits”), 31, 46 (“several asserted claims do recite that the ‘transaction’ includes ... ‘address and data bits of [a] (PCI) bus transaction’”). The Federal Circuit expressly held the District Court “was correct in treating these related terms similarly,” including a claim reciting “wherein the serial bit stream of PCI bus transaction comprises encoded PCI *address and data bits*,” whereas other terms did not recite specific bits. *ACQIS, LLC v. EMC Corp.*, No. 2021-1772, 2022 WL 1562847, at \*1 (Fed. Cir. May 18, 2022 (“*EMC Fed. Cir. Op.*”). ACQIS’s attempt to rewrite history should be rejected.

ACQIS argues the *EMC* courts did not consider Figure 8B, which depicts “the invention’s interface channel connected directly to a chip without a parallel PCI bus” and purportedly constitutes a difference in the intrinsic evidence. Resp. Br., 4. While the relevance of this Figure 8B to the PCI bus claims is less than clear, ACQIS already presented this argument to the *EMC* courts using a closely related figure. Ex. 60 (ACQIS Resp. CC Br. in *EMC*) at 4-5 (“[The system] could provide communication between conventional PCI buses, or it could provide communication directly between components, eliminating the need for an intervening PCI bus. ... Figure 8 of the ’873 patent illustrates the latter embodiment.”), 17 (“EMC’s construction would exclude the embodiment disclosed in Figure 8 and is, therefore, incorrect.”); *see also* Ex. 59 (ACQIS Corrected App. Br.) at 13-14, 47 (“[A]s shown in Figure 8 of the ’415 Patent, PCI components connect directly to interface controllers, or through other bus types, without any intervening PCI Local Bus.”). Moreover, the Asserted Patents are undoubtedly continuations of, and related to, the ’873 and ’415 Patents at issue in *EMC*.<sup>2</sup> The intrinsic evidence is the same in this case as in *EMC*.

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<sup>2</sup> Indeed, ACQIS has argued before the PTAB that its patents including Figs. 8A-8B were incorporated by reference into the Asserted Patents, such as the ’750 Patent. *See* Ex. 61 (ACQIS Prel. PO Resp.) at 6-10 (noting that “each subsequent application in the ’750 patent’s priority chain included the same figures and disclosure,” including that “Figures 8A and 8B are from Chu ’886,” and the “incorporation by reference of Chu ’886 into Chu ’330”). The PTAB accepted these arguments in denying institution. Ex. 62 (Institution Decision) at 8-12.



As ACQIS acknowledges, “[t]he same claim term in the same patent or *related patents carries the same construed meaning*.” Resp. Br., 6 (quoting *Rambus*). ACQIS’s quotations from *SightSound* and *Abtox* similarly recognize common terms across related patents must be construed the same. *Id.* There can be no dispute that the Asserted Patents are “related” to those in *EMC*.

Finally, ACQIS argues that these claim scope issues were not actually litigated in *EMC* because the District Court only “determine[d] that the phrase does not require a physical PCI bus.” Resp. Br., 7. ACQIS notes that certain constructions were stipulated and purportedly should not be afforded preclusive effect. However, the main case cited by ACQIS for this proposition considered a stipulation that “specifically stated that it was for the purposes of that litigation only” and that it was not a final judgment. *Pfizer, Inc. v. Teva Pharms. USA, Inc.*, 429 F.3d 1364, 1375-76 (Fed. Circ. 2005) (noting that stipulated construction from prior case “specifically stated that it was for the purposes of that litigation only”). *Allergan* is not applicable because it did not involve constructions “expressly adopted” by the Federal Circuit, and, as discussed herein, the issues surrounding the PCI bus transaction terms were actually disputed and litigated throughout *EMC*.

Accordingly, the Court should preclude ACQIS from arguing for constructions different than those expressly adopted by the Federal Circuit.

## II. DISPUTED CLAIM TERMS

### A. “low voltage differential signal (LVDS) [channel]” / “LVDS [channel]”

ACQIS argues that LVDS was so well-known at the time of invention that it had a “generic, objective meaning to a POSITA.” Resp. Br., 9. ACQIS is correct that “LVDS” was well-known and had an objective meaning, but it is not some nebulous, undefinable “generic meaning.” LVDS is a standard that, not surprisingly, is defined by standards documents. ACQIS told a prior court exactly the same thing—namely there are “*several prior art references* [cited by the Patents-in-Suit] *that define LVDS*.” Dkt. 53-27 at 7. In particular, ACQIS cited the same TIA/EIA-644

standard in Defendants’ construction and the “Overview of LVDS Technology” that expressly “*define[s] LVDS*” with the same two standards in Defendants’ construction. Dkt. 53-27 at 8. ACQIS offers no rationale to explain why LVDS is not defined by these LVDS standards.

ACQIS attempts to distance itself from the well-known LVDS standard by twisting the specification’s teaching that LVDS is used “to generically refer to low voltage differential signals and is not intended to be limited to any particular type of LVDS technology.” ’750 Patent at 4:11-18. LVDS is a generic standard, defining a broad class of technology, that can be implemented in a variety of ways consistent with the LVDS standard. There are many known species of LVDS compliant technology. An example of a species proffered by the specification is Silicon Image’s<sup>3</sup> proprietary PanelLink technology called TMDS. *Id.* at 21:29-34. Other examples are the VESA P&D standard and DVI Specification (*see* Resp. Br., 10-11), which relate to two other species of LVDS-compliant technologies.<sup>4</sup> The fact these standards provide additional requirements for certain applications does not mean that LVDS is not itself a standard. Whether a particular standard is a variant of LVDS can be determined by simply comparing it to the LVDS standard. If it is compliant with the LVDS standard (even if it has additional requirements), it is a species of LVDS. If it is not compliant with the LVDS standard, it is not a species of LVDS.

ACQIS’s arguments are inconsistent with its own claiming paradigm. Specifically, some limitations claim in non-standards-based terminology (e.g., “differential signal channel(s)”) while

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<sup>3</sup> It is worth noting Silicon Images, in its own patents, defines “LVDS” with reference to the same standards used in Defendants’ construction. Ex. 63, U.S. Patent No. 7,502,411 at 3:24-29 (Other serial links include the set of serial links known as *Low Voltage Differential Signaling (“LVDS”) links* (e.g., “LDI,” the LVDS Display Interface), *each of which satisfies the TIA/EIA-644 standard or the IEEE-1596.3 standard[.]*”); Ex. 64, U.S. Patent No. 7,558,326 at 5:7-11 (defining “LVDS” similarly). This is further evidence a POSITA would have understood LVDS is defined by standards and is not a “generic” technology.

<sup>4</sup> ACQIS also relies on materials relating to a technology called HyperTransport. However, as ACQIS recognizes, HyperTransport is “not the conventional *LVDS standard*,” but an “enhanced LVDS technique” that uses a “driver supply voltage [of] 1.2 volts, instead of the conventional 2.5 volts for standard LVDS.” Resp. Br., p. 11. In other words, HyperTransport is not LVDS.

others claim specific standards (e.g., LVDS or TMDS).” *See, e.g.*, ’750 patent, claims 10, 12, 24, 35; ’140 patent, claims 14-15, 18, 21, 30-31, 34-36, 38. ACQIS knew full well how to claim a differential signaling technology without referencing a standard and did so when it claimed “differential signal channels.” In numerous other claims, however, ACQIS intentionally recited a standard, and the claimed standard necessarily applies to define the claim scope. The same is true when comparing claims that recite differing standards, e.g., TMDS and LVDS. Some claims use one standard and some the other. This is intentional because TMDS has additional requirements over LVDS that suit it for the context of claims in which it appears. ACQIS was deliberate in its claiming, using non-standards-based language (“differential signal channels”) where intended and using specific standards (LVDS, TMDS, PCI, and USB) when it intended to claim those standards.

ACQIS chides Dr. Wolfe for not specifically citing the portion of the specification stating TMDS is Silicon’s Images’ version of LVDS technology. Dr. Wolfe fully considered the teachings of the specification. He expressly noted the portion that references LVDS as being a “generic technology” and “not limited to any particular type of LVDS technology” (Dkt. 53-20, ¶40). As noted above, LVDS is a class of technology defined by the LVDS standards and should not be limited to any type or species of LVDS-technology. ACQIS, in contrast, is trying to read out its decision to claim the LVDS standards by name.

Knowing that objectively defining LVDS apart from an associated standard is flatly impossible, ACQIS strangely attempts to define the LVDS standard with reference to two other random (or at least cherry-picked) differential signaling standards. Specifically, ACQIS argues that “LVDS refers to a differential signaling technique that allowed a voltage swing lower than prior data transmission standards, such as ECL and PECL.” Resp. Br., 9-10 (relying on Sarhan Decl., ¶42). The irony is apparent. ACQIS is arguing that LVDS should not be defined by the

actual LVDS standards that existed at the time, but instead should be defined relative to two other standards. This defies logic when there is—in ACQIS’s own words—a “well known” standard that “define[s] LVDS.” Even ACQIS’s expert, Dr. Sarhan, concedes that LVDS “*could be used to refer to a specific standard.*” Dkt. 54-2 (Sarhan Decl.), ¶32. Indeed, Dr. Sarhan relies on the same “Overview of LVDS Technology” that states “there are *two industry standards that define LVDS*” to support that LVDS simply means lower than PECL and ECL. *Id.*, ¶42.

It is not clear why ACQIS chooses PECL or ECL as reference points instead of numerous other differential signaling standards that existed at the time. Cherry-picking usually targets a sweet spot. But putting aside the cherry-picking, referencing two other standards to define LVDS does not define LVDS with any degree of certainty. How much lower does the “voltage swing” need to be than that in PECL or ECL? What other “prior data transmission standards” could it be lower than? And if some of the “prior data transmission standards” are higher than ECL and PECL, does that mean ECL and PECL are also LVDS because they are lower than other “prior data transmission standards”? And how does the “low voltage,” not the “voltage swing,” carried by the lines factor into whether it is LVDS, as ACQIS previously alluded to (*see* Dkt. 53-27 at 8) and appears to also currently contend is relevant to the inquiry (*see* Resp. Br., 13 (“‘LVDS’ utilized lower voltage than existing data transmission techniques[.]”)). These are just a few of the problems with ACQIS’s proffered “objective boundary.” Resp. Br., 13. ACQIS’s proposal seems like a long journey for a short trip. There are LVDS standards that indisputably define LVDS and those are the objective boundary for LVDS. The LVDS standards identified in Defendants’ construction provide the only objective boundary for LVDS known to a POSITA at the time of the inventions. *See* Dkt. 53 at 6 (citing *BillJCo*, *ACQIS v. Samsung*, *Fundamental Innovation Sys.*, and *Uniloc*). Without the standards, LVDS has no objective, definable meaning and is indefinite.

**B. “Peripheral Component Interconnect (PCI) [/PCI] bus transaction”**

The Federal Circuit limited a “PCI bus transaction” to a transaction “in accordance with the industry standard PCI Local Bus Specification.” *ACQIS, LLC v. EMC Corp.*, 2017 WL 6211051, at \*5, 8 (D. Mass. Dec. 8, 2017) (“*EMC Markman*”); *EMC Fed. Cir. Op.*, 2022 WL 1562847, at \*1; Dkt. 53-44 at 17-18. ACQIS’s proposed modification to this term is inconsistent with the Federal Circuit’s construction because it adds a second, *alternative*, category of transactions to that construction: a transaction [1] in accordance *or [2] backwards compatible* with the industry standard PCI Local Bus Specification. While ACQIS argues that the Court’s prior construction is consistent with the Federal Circuit’s construction (Resp. Br., 15-16), it knows this is not true because “*or backwards compatible*” is expressly written as an alternative. Recognizing that this construction is incorrect on its face, ACQIS now, for the first time, says that it “**would be appropriate to adopt the construction that excludes ‘or backward compatible’**” but provide further clarification.” Resp. Br., 16. ACQIS knows the construction using “or backwards compatible” is not consistent with settled Federal Circuit law and will not withstand an appeal. Further, ACQIS’s suggestion that the Court provide a “clarification” is expressly inviting the Court to commit the same error that ACQIS recognizes in its own proposed construction. The Court should not allow such posturing and should simply adopt the Federal Circuit’s construction as Defendants, and now ACQIS, propose. Indeed, the court must adopt it as it is settled law subject to preclusive effect.

Despite this, ACQIS repeatedly states that “adding ‘backwards compatibility’ does not expand the claim scope.” Resp. Br., 14-17 (citing to Ex. 54, *ASUSTeK*, Dkt. 124 (Transcript of Sept. 1, 2022 Hearing) at 36:6-16). But if this were true, there would be no need to include it or “clarify” the construction at all. Regardless, if ACQIS believed that “backwards compatible” means that it “allows compatibility with PCI legacy devices” (Resp. Br., 17), it should have included such language in its construction. But it failed to do so. The addition of the alternative

“or backwards compatible” necessarily assumes the possibility of including other transactions not in “accordance with the PCI Specification.” This completely contradicts the Federal Circuit’s construction. *See, e.g., Eolas Techs., Inc. v. Adobe Sys., Inc.*, No. 09-CV-446, 2011 WL 11070303, at \*2 (E.D. Tex. Sept. 23, 2011) (acknowledging Federal Circuit constructions as binding).

ACQIS’s construction is also inconsistent with and not supported by the intrinsic record. Ex. 37, ¶37. Indeed, ACQIS admits that “the words ‘backwards compatible’ do not appear in the Asserted Patents,” yet maintains it is consistent with the intrinsic record. Resp. Br., 16. ACQIS relies on the lack of a PCI bus in certain embodiments and its expert’s interpretation of alleged advantages of the claimed invention as “intrinsic evidence” supporting its construction. However, an expert declaration is not “intrinsic evidence.” To support its argument, ACQIS points to figures that “have no parallel PCI bus and replace that architecture with a serial architecture.” Resp. Br., 17. As discussed in Section I, this argument was already considered in the *EMC* case. It is also not surprising that the specification describes an embodiment without a PCI bus because certain claims have no language relating to a PCI bus transaction at all. *See, e.g.,* ’750 Patent, claims 24, 48, 50; ’768 Patent, claim 36; ’797 Patent, claims 27, 30, 33; ’140 Patent, claims 14, 18, 22, 26, 35; ’654 Patent, claim 20. Regardless, where the claims recite a “PCI bus transaction,” there must be a “a transaction, in accordance with the industry standard PCI Local Bus Specification.”

Finally, ACQIS argues its “statements to the PTAB have no bearing on the inclusion of ‘or backwards compatible’ in the construction of ‘PCI bus transaction.’” Not so. If ACQIS believed “backwards compatible” was within the scope of “PCI bus transaction,” surely it would have argued as much in the IPR. Regardless, ACQIS made repeated, unequivocal statements as to what it believed “PCI bus transaction” means and even agreed to Defendants’ construction in prior litigation without any mention of “backwards compatible.” *See* Dkt. 53 at 12-14. Accordingly,

ACQIS should be held to its prior statements and the Court should adopt Defendants’ construction.

C. **“convey [/conveying/conveys/communicating/communicate/transmitting] ... a Peripheral Component Interconnect (PCI) bus transaction”**

ACQIS once again misrepresents the record before the Federal Circuit when it argues that “[u]nlike the claims addressed substantively in *EMC*, ... every Asserted Claim that references a PCI bus transaction specifies the bits *actually conveyed*[.]” While every claim in *EMC* may not have recited specific bits, ACQIS cannot contest that there were claims at issue in *EMC* that recited specific bits. Indeed, ACQIS’s claim construction briefing in *EMC* recognized as much.” *See* Dkt. 53-38 (Ex. 38) at 21; Ex. 60 (ACQIS Resp. CC Brief in *EMC*) at 23 (“*EMC*’s proposed construction [of ‘communicating’ terms] contradicts several asserted claims, which require the communication of ‘address and data bits of PCI bus transaction’ without referencing other information, such as PCI command codes.”); *see also EMC Fed. Cir. Op.*, 2022 WL 1562847, at \* 1, fn.1 (noting it is appropriate to treat claims similarly, including those reciting “communicating ... encoded PCI address and data bits”). This defeats any distinction ACQIS is trying to make.

ACQIS also presented this exact issue on this same claim language to the Federal Circuit, noting that “[t]he parties did not agree on a construction for the related phrase ‘communicate address and data bits of [a] PCI bus transaction,’ and similar variations, as recited in the Address and Data Claims.” Ex. 59 (ACQIS Corr. Appeal Br.) at 26-27; *id.* (arguing that, even if a “transaction” requires physical layer signals, summary judgment would still be inappropriate against the Address and Data Claims, which explicitly recite transmitting only the “address and data bits of a PCI bus transaction.”). Specifically, ACQIS “argued that these claims could not require transmitting the address and data bits *and also the control bits*, because that would contradict those claims’ language.” *Id.*; *see also id.* at 53-55 (noting “the Address and Data Claims” “only required communicating the address and data bits,” but the “district court granted

summary judgment of non-infringement against those claims anyway.”). Thus, even though specific bits were recited in the claims in *EMC*, the District Court and Federal Circuit found that “communicating” a “PCI bus transaction” requires communication of “all address, data, and control bits.” These facts defeat the underlying premise of ACQIS’s argument.

ACQIS further suggests that statements made in the IPR should not apply to claims reciting specific bits because “ACQIS’s IPR counsel was referring to ’873 claim 54 (or in some instances, dependent claim 61), which requires conveying an entire PCI bus transaction and not specific, recited bits like the Asserted Claims.” Resp. Br., 20. This is plainly false. Claim 61 of the ’873 Patent specifically recites: “[t]he computer module of claim 54, wherein the [communicated] encoded serial bit stream of PCI bus transaction comprises encoded PCI *address and data bits*.” Dkt. 53-10 at 44:5-7. And in this context, ACQIS’s IPR counsel argued: “*[T]here is no such thing as a PCI transaction that does not have control bits. To carve control bits out of claim 54 and 61 is to make sure it does not comply with either the standard of a PCI or the purpose of the invention.*” Dkt. 53-36 at 38:7-17; *see also* Dkt. 53 at 15-18.<sup>5</sup> ACQIS’s remaining arguments about control signals and the corresponding scope of the claims in *EMC* were similarly made by ACQIS and rejected by the Federal Circuit. *See* Ex. 59 (ACQIS Corr. App. Br.) at 27-28, 30, 49-51, 57-61. Accordingly, the Federal Circuit’s express construction should be adopted.

**D. “of a Peripheral Component Interconnect (PCI) bus transaction”**

ACQIS’s Response demonstrates another obvious attempt to read “PCI bus transaction” out of claims expressly reciting “PCI bus transaction.” ACQIS argues Defendants’ proposed construction is “unnecessary and incorrect” because it purportedly removes the context of the

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<sup>5</sup> ACQIS references Judge Davis’s note regarding claim 61. Dkt. 54 at 20 fn.7. This note was made before the Federal Circuit affirmed and adopted the *EMC* District Court’s constructions, which was based on these same statements relating to claim 61, and other claims reciting communicating specific bits of data.



recited bits. Resp. Br., 23. ACQIS argues the claims only require conveyance of the recited bits, “regardless of those bits’ origin.” *Id.* It is illogical to suggest that specifically recited bits “of a PCI bus transaction” do not need to be “from a” PCI bus transaction. Using ACQIS’s logic, any transaction could qualify as a PCI bus transaction. ACQIS does not point to any evidence to support its argument. Defendants’ construction should be adopted.

**E. Claims reciting a PCI bus transaction, or an encoded PCI bus transaction, “in [a] serial form” or “serially encoded” or “in a serial bit stream”**

ACQIS once again mischaracterizes the claims at issue in *EMC* as being directed to “a complete [PCI bus] transaction,” as opposed to being directed to “specific bits of a PCI bus transaction.” Resp. Br., 25. As discussed in Section I, the claims at issue in *EMC* undeniably included claims reciting “specific bits of a PCI bus transaction.” Putting that falsehood aside, it has no relevance to the real dispute here, which is whether the term “encoded” had any significance to the *EMC* District Court’s construction, and Federal Circuit’s adoption of the same, that a PCI bus transaction is serialized from a parallel form. Moreover, although the *EMC* court’s ruling applies to terms that include an “encoded” PCI bus transaction but do not specifically recite a “serial” form, the underlying rationale applies equally to claims that recite a “serial” PCI bus transaction but not “encoded,” because the *EMC* court’s construction was based on intrinsic evidence demonstrating that a “serial” PCI bus transaction necessarily requires conversion from the standard parallel form. *See, e.g., EMC Markman*, 2017 WL 6211051, at \*7 (“The claim language and specification, when read in context with the industry standard, support the construction that a PCI bus transaction is in a parallel form prior to being serialized.”). ACQIS does not dispute that the *EMC* Court’s construction and finding of disclaimer relating to this term had nothing to do with the word “encoded.” This is apparent from the specification’s description of serializing separate from the description of encoding. *See* Dkt. 53 at 22-27. This is also apparent

from ACQIS's proposed construction of "encoded," which has nothing to do with "serializing." ACQIS does not even attempt to address these facts.

ACQIS also argues a "PCI bus transaction need not originate in parallel form," but does not point to any express disclosure of this concept in the specification. Instead, it points generally to Figures 8A and 8B<sup>6</sup> which purportedly "depict embodiments corresponding to the Asserted Claims here" that "illustrate a serial LVDS channel direct from a chip with no parallel PCI bus, and therefore no need for any PCI bus transaction ... to originate in parallel form." Resp. Br., 25. ACQIS ignores the fact that each Asserted Patent includes independent claims (some of which are asserted) that are directed to LVDS channels and that do not recite a "PCI bus transaction." '750 Patent, claims 24, 48, 50; '768 Patent, claim 36; '797 Patent, claims 27, 30, 33; '140 Patent, claims 14, 18, 22, 26, 35; '654 Patent, claim 20. Figures 8A and 8B depict such an embodiment. These figures do not reference a PCI bus transaction at all and, therefore, do not support ACQIS's argument that a "PCI bus transaction" need not be serialized from a parallel form.

ACQIS does not otherwise address the plethora of statements in the prosecution history describing the "whole point" of ACQIS's invention was to "serialize the otherwise parallel PCI bus transactions." Dkt. 53 at 24-26. Nor does ACQIS address the fact that it already challenged and lost its objections to this construction before the Federal Circuit. *See* Ex. 59 (ACQIS Corr. App. Br.) at 62 ("The Court should vacate the erroneous construction of 'encoded ... (PCI) bus transaction.'"). Accordingly, the Court should adopt Defendants' construction.

#### **F. "console"**

ACQIS again tries to distance itself from its twice-agreed construction of "console" for no

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<sup>6</sup> ACQIS also argues Figures 8A and 8B are not in the patents at issue in *EMC*. As discussed in Section I, ACQIS made the same arguments regarding similar figures in *EMC* and has also successfully argued these figures are incorporated by reference from earlier ACQIS patents.

legitimate reason. ACQIS does not argue that Defendants’ construction is incorrect or unsupported by the specification because that would be wrong. Instead, ACQIS argues the same patents were not involved in the prior case from which Defendants’ construction comes. This is disingenuous because, as discussed in Section I, ACQIS has repeatedly emphasized the familial relationships between its patents. The Asserted Patents are continuations of patents at issue in the prior *Appro/EMC* proceeding. Specifically, the ’750, ’768, and ’797 patents are continuations of the ’624 patent, and the ’140 and ’654 patents are continuations of the ’984 and ’468 patents asserted in that case. *See EDTX Markman*, 2015 WL 1737853, at \*1 (reciting asserted patents); Dkt. 53-1 through 53-5 (claiming priority to same patents). Second, the construed claim term, “console,” is identical. *EDTX Markman*, 2015 WL 1737853, at \*7 (construing “console”).

ACQIS tries to justify its proposed construction by citing the specification describing “a console comprising a first coupling site *and* a second coupling site” and that “is an enclosure that is capable of housing *each coupling site*.” Resp. Br., 27-28 (citing ’768 patent). This disclosure, describing a plurality of coupling sites, is inconsistent with ACQIS’s construction, which only requires “*one* or more coupling sites.” In fact, it supports Defendants’ construction which requires that a console “connects *several components* of a computer system.”

**G. “USB protocol” / “USB protocol data/information”**

As Defendants’ construction makes clear (and the *Samsung* decision confirms (Dkt. 53-21, at 31-33)), the USB protocol terms are properly construed with reference to the USB 2.0 Specification—the version of the protocol existing at the time of the patent application filing. The USB 2.0 Specification is intrinsic evidence on the face of the patents, and it is how a POSITA would understand the USB protocol terms. Dkt. 53-37, ¶ 41.

ACQIS first attacks a strawman that Defendants’ construction does not require – that the claims do not recite a USB bus and “all the aspects required to implement such a bus.” Resp. Br.,

28. Rather, Defendants contend, and the USB 2.0 Specification makes clear, that the USB protocol requires more than communicating some *data* or *information*. It requires communications compliant with the standard, and nothing in the intrinsic record justifies ignoring the plain meaning of the USB protocol terms to require some arbitrary subset of the USB protocol.

ACQIS argues no construction of the USB terms is needed and that the “phrases should be given their plain and ordinary meaning.” Resp. Br., 28. But ACQIS’s arguments illustrate exactly why these terms should be construed. For example, ACQIS argues the claims “do not require every aspect of the USB specifications,” but then limits the claimed “USB information” to only “data” and “data payload.” *Id.*, 28-29. There is nothing in the claims or patent specifications that support limiting the relevant USB specifications to narrow slices of “data” or “data payload,” especially given ACQIS has not proposed any construction including these requirements. Indeed, the USB 2.0 Specification explains that the “protocol” is a “specific set of rules, procedures, or conventions relating to *format and timing of data transmission* between two devices,” not just data. Dkt. 53-46 (Ex. 46) at 8. Accordingly, Defendants’ construction is correct and should be adopted.

ACQIS’s attempts to distinguish *Fundamental* and *Uniloc* fail.<sup>7</sup> ACQIS argues *Fundamental* does not apply because the claims “explicitly depart from the teachings of USB at the time.” Resp. Br., 29-30. ACQIS bases this allegation on *other* claim terms (e.g., unidirectional, serial channels, etc.), not the USB terms being construed. *Fundamental* focused on how the USB terms were claimed and described in the specification, not by how they related to other claim terms. *Fundamental Innovation Sys. Int’l LLC v. Samsung Elecs. Co.*, 2018 WL 647734, at \*7-11. Here, it is undisputed that USB 2.0 and prior versions were the only specifications existing at the time,

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<sup>7</sup> Despite repeatedly citing to the *Samsung* case for the PCI terms, ACQIS fails to acknowledge that *Samsung* agreed with Defendants’ USB construction, evidencing ACQIS’s pattern of ignoring statements/holdings from prior decisions that do not support its positions.

with USB 2.0 being specifically mentioned in the asserted patents (e.g., '768 patent at 12:16-17). *Uniloc* also does not contradict Defendants' construction because if the same protocols required by USB 2.0 are also required by USB 3.0, it is possible that it is within scope, assuming it satisfies other requirements of the claim language. It is indisputable, however, that a POSITA could not have understood claims to encompass something that did not exist until years later. *Fundamental Innovation*, 2018 WL 647734, at \*9-11 ("An invention cannot comply with standards not yet in existence."); *Uniloc USA, Inc. v. Apple, Inc.*, 2021 WL 432183 at \*8 (N.D. Cal. Jan. 15, 2021).

#### **H. serial bit channels and "serial channel"**

ACQIS does not contend Defendants' proposed construction is incorrect or not supported by the specifications. Nor could it because it previously agreed to the same construction. Instead, ACQIS argues these are "different claims and patents," which is not accurate because the '750, '768, and '797 patents are continuations of the '624 patent asserted in that case, and the '140 and '654 patents are continuations of the '984 and '648 patents asserted in that case. *See EDTX Markman*, 2015 WL 1737853, at \*1 (reciting asserted patents); Dkt. 53-1 through 53-5 (claiming priority to same patents). Second, the claim terms are identical. *EDTX Markman*, 2015 WL 1737853, at \*3 (reciting agreed constructions for "serial bit channel" and "serial ... channel"). Like terms from patents in same family should be construed similarly. *See In re Rambus Inc.*, 694 F.3d 42, 48 (Fed Cir. 2012); *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1334 Fed. Cir. 2003. ACQIS also argues its prior construction introduced a "new limitation" and used a word, "component," that introduces ambiguity. Resp. Br., 30. There is no evidence or argument as to how the word "component" is ambiguous or why a new limitation is introduced. A "channel" does not exist in isolation—it connects two things—and in the context of the claims, it does so to transmit information serially (and in opposite directions) from one thing to another.

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Respectfully submitted,

/s/ Mark C. Lang

Eric A. Buresh

Mark C. Lang (Pro Hac Vice)

7015 College Blvd, Suite 700

Overland Park, KS 66211

Email: eric.buresh@eriseip.com

Telephone: (913) 777-5600

Facsimile: (913) 777-5601

Abran J. Kean (Pro Hac Vice)

5299 DTC Blvd., Suite 1340

Greenwood Village, CO 80111

Email: abran.kean@eriseip.com

Telephone: (913) 777-5600

Facsimile: (913) 777-5601

Melissa Smith

Texas State Bar No. 24001351

melissa@gillamsmithlaw.com

GILLAM & SMITH, L.L.P.

303 South Washington Avenue

Marshall, Texas 75670

Telephone: 903-934-8450

Facsimile: 903-934-9257

*Counsel for Defendants Sony Interactive  
Entertainment LLC and Sony Interactive  
Entertainment Inc.*

**CERTIFICATE OF SERVICE**

The undersigned hereby certifies that a true and correct copy of the above and foregoing document has been served on June 23, 2023, to all counsel of record who are deemed to have consented to electronic service via the Court's CM/ECF system.

/s/Mark C. Lang  
Mark C. Lang